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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER |
|---|
| FERRIS III, FRED O |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 08/13/2003

10

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/328,800 | ITO ET AL. | |
| | Examin r | Art Unit | |
| | Fred Ferris | 2123 | |

*-- The MAILING DATE of this communication app ars on the cover sh et with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

*1. Claims 1-23 have been presented for examination based on applicant's amendment filed on 21 May 2003 (paper #9). Claims 1-23 remain rejected by the examiner.*

### *Response to Arguments*

*2. Applicants arguments filed on 21 May 2003 (paper #9) have been fully considered.*

*Regarding applicant's response to objection to claim 19: Applicants have amended claim 19 to overcome objection to the claim. Examiner withdraws the objection to claim 19.*

*Regarding applicant's response to 112(1) rejection of claims 16 and 19: Applicants have sufficiently amended claims 16 and 19 to overcome 112(1). Examiner withdraws the 112(1) rejection of claims 16 and 19.*

*Regarding applicant's response to 102(b) rejection: Applicants have argued that Huang does not disclose emulation features where part of the logically equivalent functions to be developed are mounted on a logic board for verification. In response to applicant's argument that "**at least part of the logically equivalent functions to an LSI to be developed are mounted on a logic board prepared for logic verification**" a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of*

*performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963). Huang clearly discloses an emulation system used for design verification as cited in the previous office action. Further, the Inchoate ASIC of Huang is merely defined as an ASIC (LSI) that has been designed but not yet fabricated (i.e. equivalent to the LSI to be developed of the claimed invention) and requires testing for verification purposes. (CL3-L54, CL9-L65) Hence, Huang can obviously perform verification of equivalent functions of the design. Writing of the functionally equivalent logic data to the target would also obviously be inherent in Huang.*

*Applicants further argue that prior art does not disclose providing the logically equivalent function without using any special parts or external systems to enable short term and low cost verification. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the feature upon which applicant relies (i.e., providing the logically equivalent function without using any special parts or external systems to enable short term and low cost verification) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further, applicants appear to be attempting to argue the specifications definition of certain claimed limitations such as the "**terminal land** for supporting an LSI targeted for development*

*and mounted on the board" which the examiner interprets a being equivalent to the socket (CL12-L15) disclosed by Huang.*

*Applicant's have also argued that Huang does not disclose wiring that includes lines for directly coupling the connectors to programmable LSI's and for linking connectors by way of switching LSI's. The examiner asserts that this feature is obviously inherent in Huang since figures 3a and 3b clearly disclose bus connections between the programmable/switching LSI's (i.e. the FPGA's) and the connectors.*

*Accordingly, the examiner maintains the 102(b) rejection of claims 1-21.*

*Regarding applicant's response to 102(a) rejection of claims 22 and 23: The examiner withdraws the 102(a) rejection of claims 22 and 23 based on amended claims. However, the examiner has applied new 103(a) art rejections to claims 22 and 23. (please see new 103(a) rejections below)*

***Claim Interpretation***

*3. The claimed invention is disclosed to be a logic module used for logic emulation and verification of electronic circuits. The device falls into the broad category known in the art as circuit emulators and in-circuit emulators (ICE). The logic module (a circuit board) contains numerous programmable large scale integrated circuits (LSI's), programmable cross-point-switches (allowing programmable connections between LSI's), and connectors for external connection and connection to an enhanced logic emulation board. A structure using popular industry techniques for multiple module staging (stacking/platform) and cooling of IC's in the structure is also described.*

## *Claim Rejections - 35 USC § 102*

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

***4. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent 5,640,337 issued to Huang et al.***

*Claims 1-9 are drawn to a* ***logic emulation module*** *comprising:*

- ***programmable LSIs*** *capable of* ***programming logic***
- ***switching LSIs*** *capable of* ***programming connections***
- ***connectors*** *for* ***external electrical connection***
- *a* ***board*** *on which to* ***mount programmable LSI's***
- ***programmable LSI's*** *and* ***connectors coupled*** *by way* ***switching LSI's***

*Per claim 1-9: Huang discloses a* ***programmable logic emulation module*** *constructed of a* ***circuit board*** *having* ***through holes*** *and* ***programmable logic devices*** *(LSI's) connected via field* ***programmable interconnect*** *(cross-point-****switches****) containing* ***connectors*** *for* ***external connection*** *used for* ***logic emulation*** *and* ***verification****. (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55)*

*Claims 10 and 11 are drawn to a* ***logic emulation board*** *comprising:*

- *connectors for connection to logic emulation* ***(additional) "stacked" module***
- ***terminal lands (pads for mounting)*** *for* ***insertion of LSI chips****.*

*Per claim 10-11: Huang discloses* ***a logic emulation board*** *that includes an* ***additional module (a "pod")*** *which can be incorporated as part of the basic* ***core-cell (module)*** *forming an equivalent pair of* ***"stacked"*** *emulation modules. The Huang device includes* ***sockets*** *for* ***insertion of LSI chips****. (CL10-L11-45, Fig. 2, 3, 5)*

*Claim 12 is drawn to a* ***logic emulation device*** *consisting of a* ***logic emulation board*** *connected to a* ***logic emulation (stacked) module*** *including:*

- ***programmable LSIs*** *capable of* ***programming logic***
- ***switching LSIs*** *capable of* ***programming connections***
- ***connectors*** *for* ***external electrical connection***
- *a* ***board*** *on which to* ***mount programmable LSI's***
- ***programmable LSI's*** *and* ***connectors coupled*** *by way* ***switching LSI's***
- ***terminal lands (pads for mounting)*** *for* ***insertions of LSI chips***

*Per claim 12: Huang discloses a* ***programmable logic emulation module*** *constructed of a* ***circuit board*** *having* ***through holes*** *and* ***programmable logic devices*** *(LSI's) connected via field* ***programmable interconnect*** *(cross-point-* ***switches****) containing* ***connectors*** *for* ***external connection*** *used for* ***logic emulation*** *and* ***verification****. Huang also discloses a logic emulation board that includes an additional module (a "pod") which can be incorporated as part of the basic core-cell (module) forming a pair of* ***"stacked"*** *modules.* ***The Huang devic includes*** *sockets for insertion of LSI chips. (CL10-L11-45, Fig. 2, 3, 5) Further, the Huang device includes*

*sockets for **insertion (and mounting)** of **additional LSI chips.** (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55, CL10-L11-45)*

*Claims 13-15 are drawn to logic module (printed circuit) board consisting of:*

- ***programmable logic** elements (with logic **data** for logic **verification**)*
- ***connectors** for exchanging **input/output** signals*
- ***switching elements** for **controlling connections** between logic elements*

*Per claim 13-15: Huang discloses a programmable logic emulation module constructed of a circuit **board** consisting of **programmable logic** elements with logic **data** for logic **verification,** connectors for exchanging input/output signals, and **switching elements** for **controlling connections** between logic elements. (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55, CL10-L11-45)*

*Claim 16 is drawn to a logic board with integrated circuits including:*

- ***terminal lands** for connecting IC's*
- ***connectors** for a logic module for **programming** IC's*

*Per claim 16: **Terminal lands** for connecting IC's and **connectors** for external connection are inherent features of nearly all logic (printed circuit) boards as well as referenced prior art. (Huang, Fig 2, 5) Further, Huang supports both on and off board **programming** of IC logic devices. (Abstract-L13)*

*Claim 17 & 18 are drawn to a **logic verification system** including a logic module implementing IC logic and a logic board carrying IC's (for undergoing logic verification) and including the features of:*

- ***programmable logic** elements (with logic **data** for logic **verification**)*
- ***connectors** for exchanging **input/output** signals*
- ***switching elements** for **controlling connections** between logic elements*
- ***terminal lands** for connecting IC's*
- ***connectors** for a logic module for programming IC's*
- ***programmed logic data** for logic verification*

*Per claim 17, 18: Huang teaches a system (including a logic "pod" module and logic board carrying IC's (undergoing logic verification)) for **logic verification** that includes all of the above listed limitations as previously discussed. Further, Huang provides a means for IC programming (on/off board) and "plug" simulation for early verification. (CL9-L65, CL-11-L23)*

*Regarding claim 19: While claim 19 is deficient and rejected under 35 U.S.C. 112(1) as previously described, the examiner makes 35 U.S.C. 102(b) rejections based on the following observations: Huang teaches **mounting** of programmable logic elements and logic "pod" module (CL12-L15, CL13-L20) and further **verification** (CL9-L65) of programmable logic IC's.*

*Regarding claims 20, 21: The teachings of Huang include the limitations of a* ***logic module*** *including* ***programmable LSI's***, ***switching IC's***, *a supporting* ***board***, *a* ***connector*** *for external signals, and* ***multiple wirings*** *between connectors and* ***programmable logic elements*** *as previously discussed. (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55)*

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

***5. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. 6,128,194 issued to Francis.***

*The factual inquiries set forth in Graham* ***v.*** *John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:*

1. *Determining the scope and contents of the prior art.*
2. *Ascertaining the differences between the prior art and the claims at issue.*
3. *Resolving the level of ordinary skill in the pertinent art.*
4. *Considering objective evidence present in the application indicating obviousness or nonobviousness.*

*Claims 22, 23 are drawn to a multiple chip circuit module (board) including:*

- ***radiation plat (heat sink)*** *over IC's*

- ***metal spacers*** *between plates*
- ***heat conduction*** *between IC's* ***radiation plate***
- ***IC's, external connectors, circuit board***

*Per claim 22, 23: Francis teaches circuit board containing multiple IC's and external connectors where the IC's are covered (top and bottom) by a heat sink (radiation plate) that is further connected to a bottom cover (heat sink) and separated by metal spacers. The IC's are mounted on heat conducting circuit board material.*

*It would have been obvious, and necessary for proper heat conduction, to conform the heat conduction shapes to the IC's, and attach the plates to four corners of the module. (Fig. 2-7, Abstract, Summary of Invention, CL2-L11, CL2-L63, CL4-L47-57, CL6-L4-20)*

## *Conclusion*

*6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly,* ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

*A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any*

*extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.*

*The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.*

*U.S. Patent 6,006,022 issued to Rhim et al teaches in-circuit emulation and verification.*

*U.S. Patent 5,331,571 issued to Aronoff et al teaches emulation of integrated circuits.*

*U.S. Patent 5,339,262 issued to Rostoker et al teaches in-circuit testing and verification.*

*U.S. Patent 5,462,442 issued to Umemura et al teaches stacked printed circuit boards.*

*U.S. Patent 5,575,686 issued to Noschese teaches stacked printed circuit boards.*

*U.S. Patent 5,574,338 issued to Babier et al teaches programmable interconnection.*

*U.S. Patent 5,748,875 issued to Tzori teaches logic simulation and emulation.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

The Official Fax Numbers are:

| | |
|---|---|
| After-final | (703) 746-7238 |
| Official | (703) 746-7239 |
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